REMARKS

Applicants' attorney would like to thank the Examiner for his helpful suggestions with respect to the claims in a telephonic interview on December 11, 2003.

In the Office Action mailed August 11, 2003:

- Claims 1-37 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
- Claims 1-7, 19 and 29-36, to the extent understood, were rejected under 35 U.S.C. 102(b) as being anticipated by the Hoeld reference (U.S. Patent 5,639,680).
- Claim 20 was indicated to be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph. Presumably, claims 21-28 that are dependent on claim 20 are also allowable.
- Claims 8-18 and 37 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, and to include all of the limitations of the base claim and any intervening claims.

With the entry of this amendment, the pending claims are 1-37.

CLAIM AMENDMENT

Claims 1, 8, 12 and 29 have been amended to specify that the logic device is operable in accordance with a plurality of input/output supply signal standards each having a specified supply signal level and at least one standard being a voltage referenced standard. This language is found in original claim 2 and has been deleted from that claim. This language supplies context for the recitation of a reference voltage and also the point of distinction from a dedicated supply signal. Additionally, claims 8 and 12 have been rewritten as independent claims that include all the limitations of their base claim, claim 1. Therefore, claim 8 and its dependent claims 9-11, and claim 12 and its dependent claims 13-18 are believed in condition for allowance.

THE REJECTIONS UNDER 35. U.S.C. 112 SHOULD BE WITHDRAWN

The Examiner contends that claim 1 is indefinite because its limitations "an input/output supply signal", on line 6, and "the reference voltage signal" at lines 1 and 3

appear to represent the same signal since the reference voltage signal is seen at the output of the switching circuit.

With this amendment, the Applicants have amended claim 1 to state that the logic device is operable in accordance with a plurality of input/output supply signal standards each having a specified input/output supply signal level and at least one standard is a voltage-referenced standard. This language is found in original claim 2 from which it has now been deleted.

As explained in the specification at page 2, lines 10-26, the reference voltage signal refers to a signal that is provided to a dedicated I/O terminal of a logic device through a switch circuit to support the device's operation according to the voltage-referenced I/O standard. However, the input/output power supply signal VCC_IO that powers both the logic device and the switch circuit is often too low to turn on the transistors in the switch circuit. Claim 1 is directed to a new switch circuit that is capable of passing a reference voltage signal to a logic device through a plurality of input buffers even though the logic device has a very low input/output power supply signal. Therefore, the reference voltage signal and the input/output power supply signal are two separate signals in the present invention.

With the amendment of claim 1 to refer to multiple input/output supply signal standards, one of which is a voltage-referenced standard, it is believed that the distinctions among the reference voltage signal, the input/output supply signal and the dedicated supply signal are now clear to one skilled in the art.

In view of the reasons above, the Applicants submit that claim 1 is definite under 35 U.S.C. 112, second paragraph.

The Examiner also contends that claims 11 and 20 appear to be misdescriptive because Fig. 1 shows that the master control signal (VREF_CONTROL) is unrelated to the logic device (140) and that the limitation "the first supply signal is a core supply signal" in claim 11 makes no sense because "the first supply signal" and "the master control signal" refer to the same entity as recited on lines 2-3 of claim 8.

Element 140 is an input buffer that supplies signals to the logic device. To clarify this, Fig. 1 has been amended as circled in red to add a box labeled "logic device". This amendment is supported by the specification at page 6, line 31. Claims 8 and 11 have been amended to delete the reference to the first supply signal and to specify in claim 11 that the logic level is determined by a core supply signal.

With these changes it is believed that the Examiner's objections to claims 11, 20 and 29 are obviated. It is to be noted that the master control signal VREF_CONTROL is

typically obtained from the logic device as stated at page 3, line 12 and page 5, lines 25-26 of the specification and that the logic level of the master control signal is specified by another signal, typically the core poser supply.

In view of the reasons above, the Applicants submit that claims 11, 20 and 29 are definite under 35 U.S.C. 112, second paragraph.

Claims 2-7, 19, 21-28 and 30-37 are dependent from the rejected claims discussed above. Therefore, they are definite under 35 U.S.C. 112, second paragraph for the same reasons their independent claims are definite under 35 U.S.C. 112, second paragraph.

With the above arguments, the Applicants have addressed the 35 U.S.C. 112, second paragraph, rejections in the Office Action mailed August 11, 2003. Therefore, the rejections should be withdrawn.

THE REJECTIONS UNDER 35. U.S.C. 102 SHOULD BE WITHDRAWN

The Examiner has rejected claims 1-7, 19 and 29-36, to the extent understood, under 35 U.S.C. 102(b) as anticipated by the Hoeld reference (U.S. Patent 5,639,680).

Hoeld teaches an input cell circuit for use in a mixed signal mode where an input pin may receive either digital or analog signals and the circuit is specifically arranged to prevent leakage current between the input of the cell and the output of the cell.

The Examiner specifically identifies the power supply VCC in Fig. 4 of Hoeld as the dedicated supply signal and contends that Hoeld has disclosed a dedicated supply signal VCC that is different from the reference voltage signal at terminal 12.

However, Hoeld does not disclose or suggest a switch circuit for providing a reference voltage signal to a logic device that is operable in accordance with a plurality of input/output supply signal standards and he does not disclose a circuit that uses a dedicated supply signal that is different from the input/output supply signal.

In view of the above-described reasons, Hoeld does not teach each of the elements recited in claim 1 and therefore claim 1 and its dependent claims 2-7 and 19 are not anticipated by Hoeld.

With respect to dependent claim 19, the Examiner contends that Fig. 1 of Hoeld shows more than one buffer coupled to the output of the switch circuit without identifying which element in Fig. 1. The Applicants assume that the Examiner refers to box 28 in Fig. 1 since this is the only element outside the input cell circuit 10. However, column 2, lines 3-4 of Hoeld only discloses that box 28 refers to a conventional analog circuit block which is the

analog portion of an integrated circuit, but does not suggest that it is an input buffer as recited in claims 1 and 19. Accordingly claim 19 is believed patentable over Hoeld.

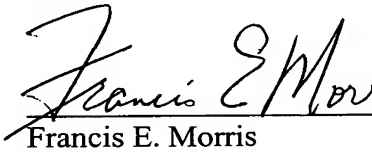
Claims 29-36 recite method/steps related to the apparatus recited in claims 1-7. Claim 29 has been amended in similar fashion to claim 1 and is believed patentable for the same reasons.

In view of the foregoing, the Applicants believe that all of the claims are now in condition for allowance and respectfully requests the Examiner to pass the subject application to issue. If for any reason the Examiner believes any of the claims are not in condition for allowance, he is encouraged to phone the undersigned attorney at (650) 849-7777 so that any remaining issues may be resolved.

Please charge any additional fee for filing this response to Pennie & Edmonds LLP's Deposit Account No. 16-1150.

Respectfully submitted,

Date: December 11, 2002



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(Reg. No.)

Francis E. Morris
PENNIE & EDMONDS LLP
1155 Avenue of the Americas
New York, NY 10036-2811
(650) 849-7777

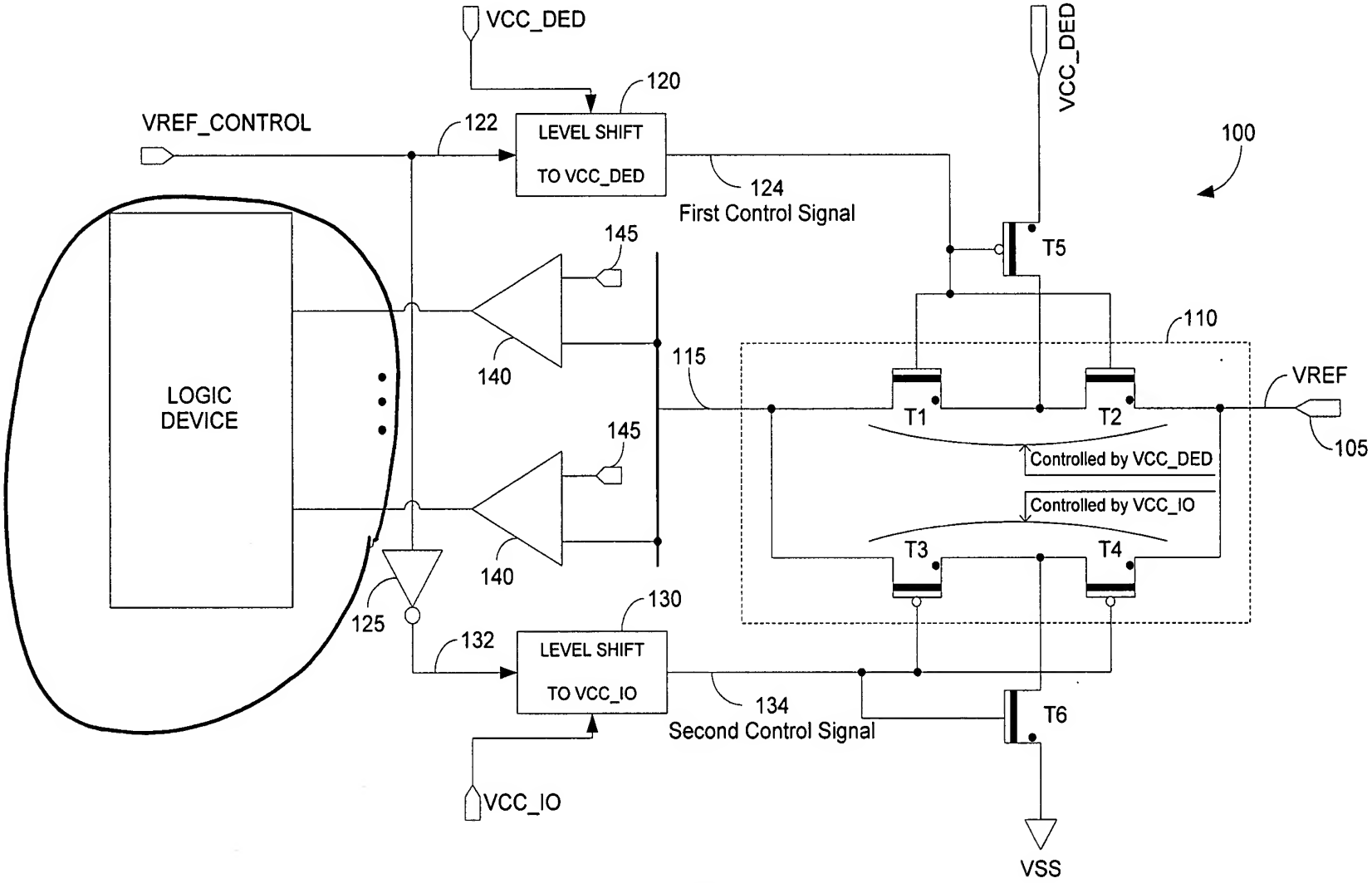

FIG. 1